Ideas for the DAQ of the DEPFET PXD

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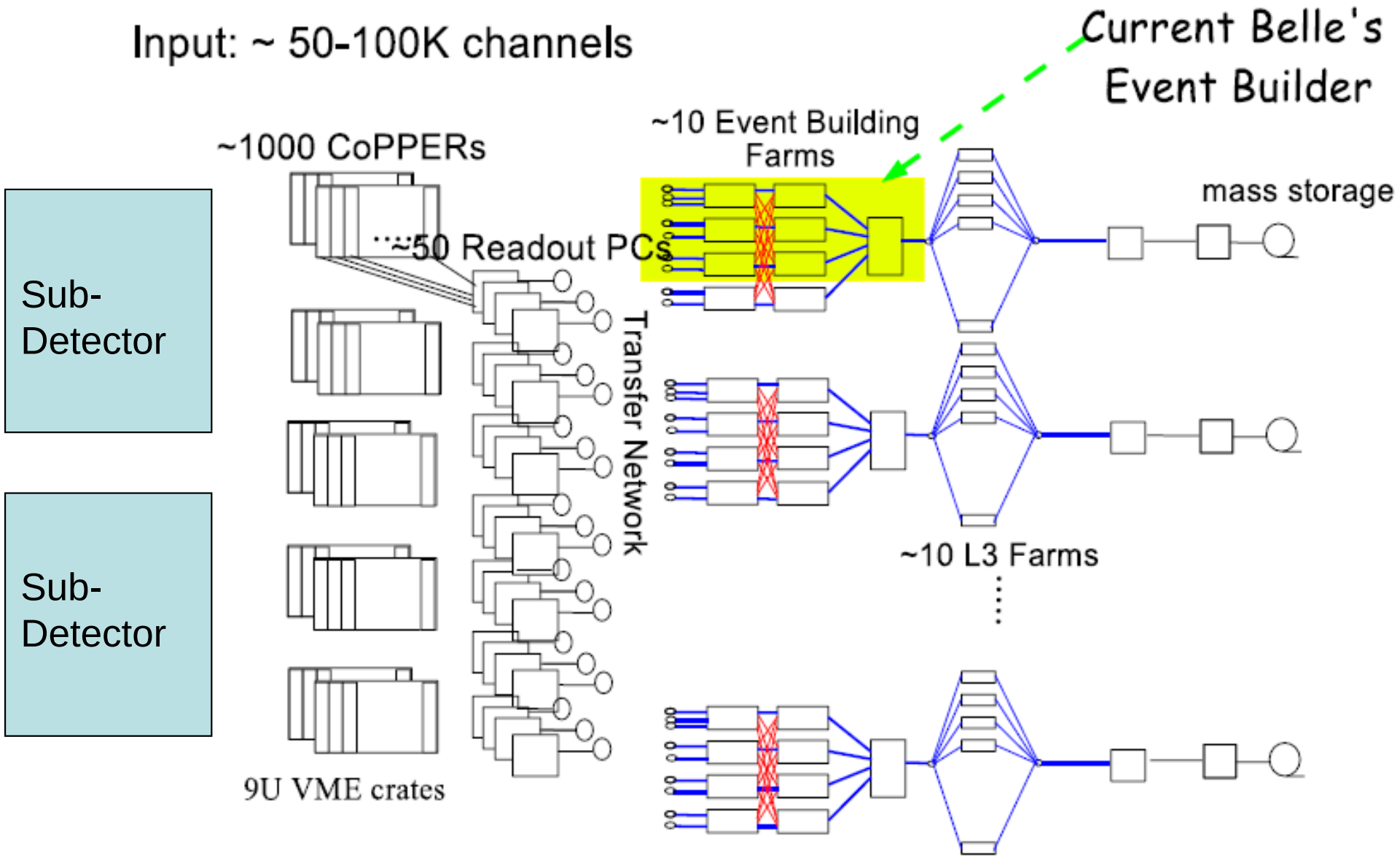
- Introduction
- PXD Data Flow & DAQ Requirements
- Proposal for the PXD-DAQ

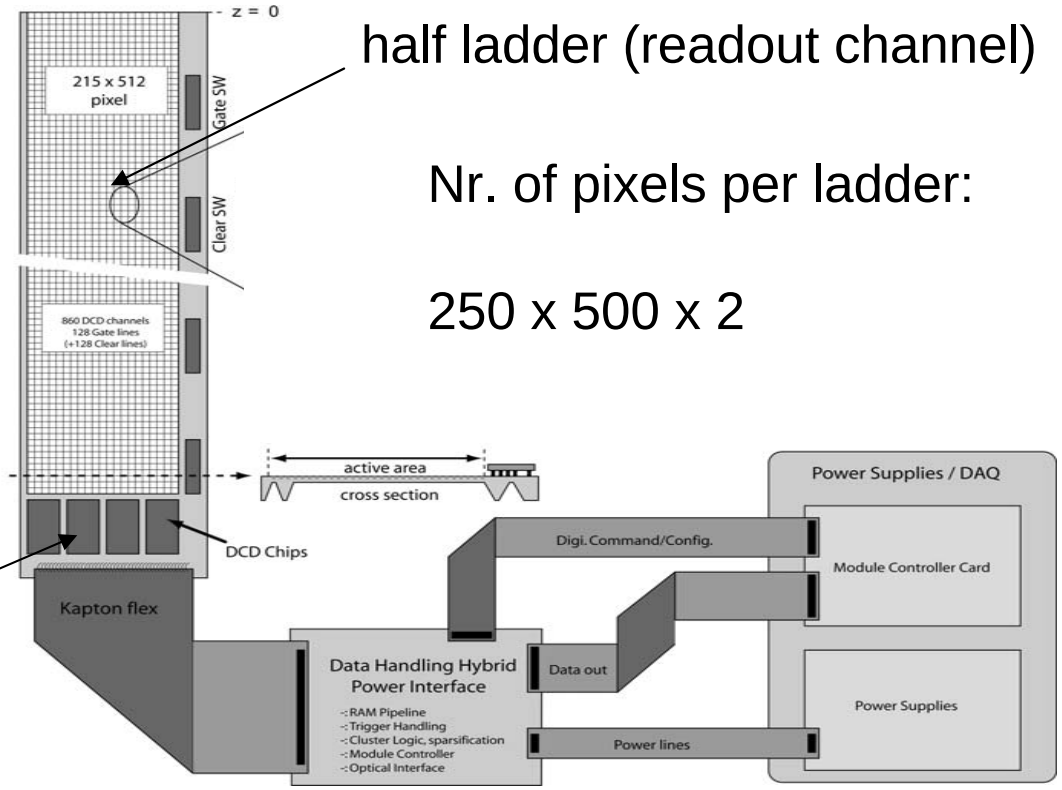
Introduction: „Current“ SuperBelle DAQ



Rate Estimates for the PXD

250

500



half ladder (readout channel)

Nr. of pixels per ladder:

250 x 500 x 2

DHP:
zero-suppression
readout buffers (10 MByte)
slow control …

DHH: module controller data link

Digitzation (DCD)

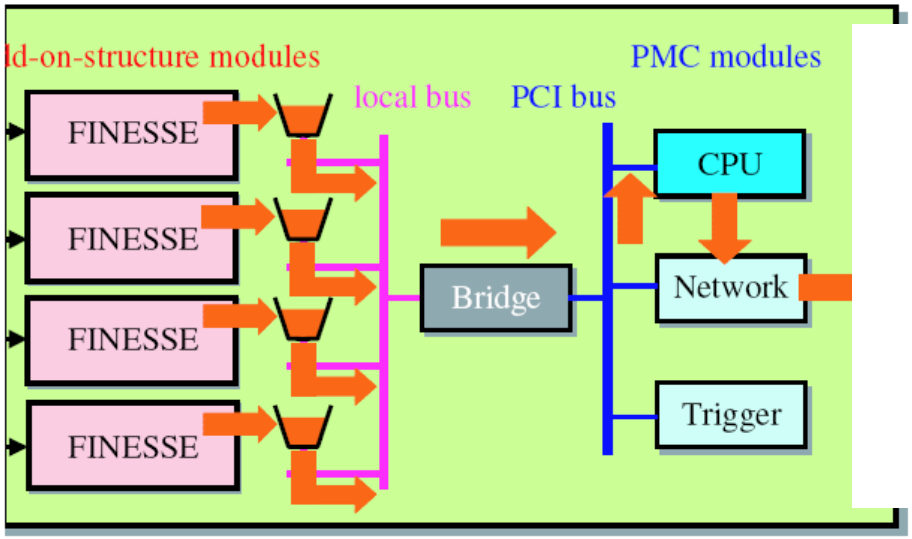
- 44 half ladders:
  5.5 Million pixels (px)
- 1-2% hit occupancy:
- 55 hits on at any time
- about 10^5 px in each event
- Trigger rate: 10-30 KHz

  Total rate: 3 x 10^9 px/s
- 4 bytes per px (pos + ADC)

Total rate: 100 GBits/s

2.5 GBits/s
per R/O channel

PXD DAQ Requirement and COPPER/FINESSE



1 R/O channel needs 2.5 Gb/s
> 11 COPPERS needed

COPPER: 133 MB/s max (PCI)

Bus too slow!

COPPER: Digitization is done on the Finesse Card
Zero-Suppression is done on COPPER CPU

But: data rate is 2 orders of magitude larger
(zero supp. only after digitization)

COPPER / FINESSE is excluded for the PXD DAQ !

The PXD DAQ Challenge

- Readout speed:

  → have to manage large (44) parallel R/O channels, each 2.5 Gb/s, total of 100 Gb/s (@ 30 kHz trigger rate)

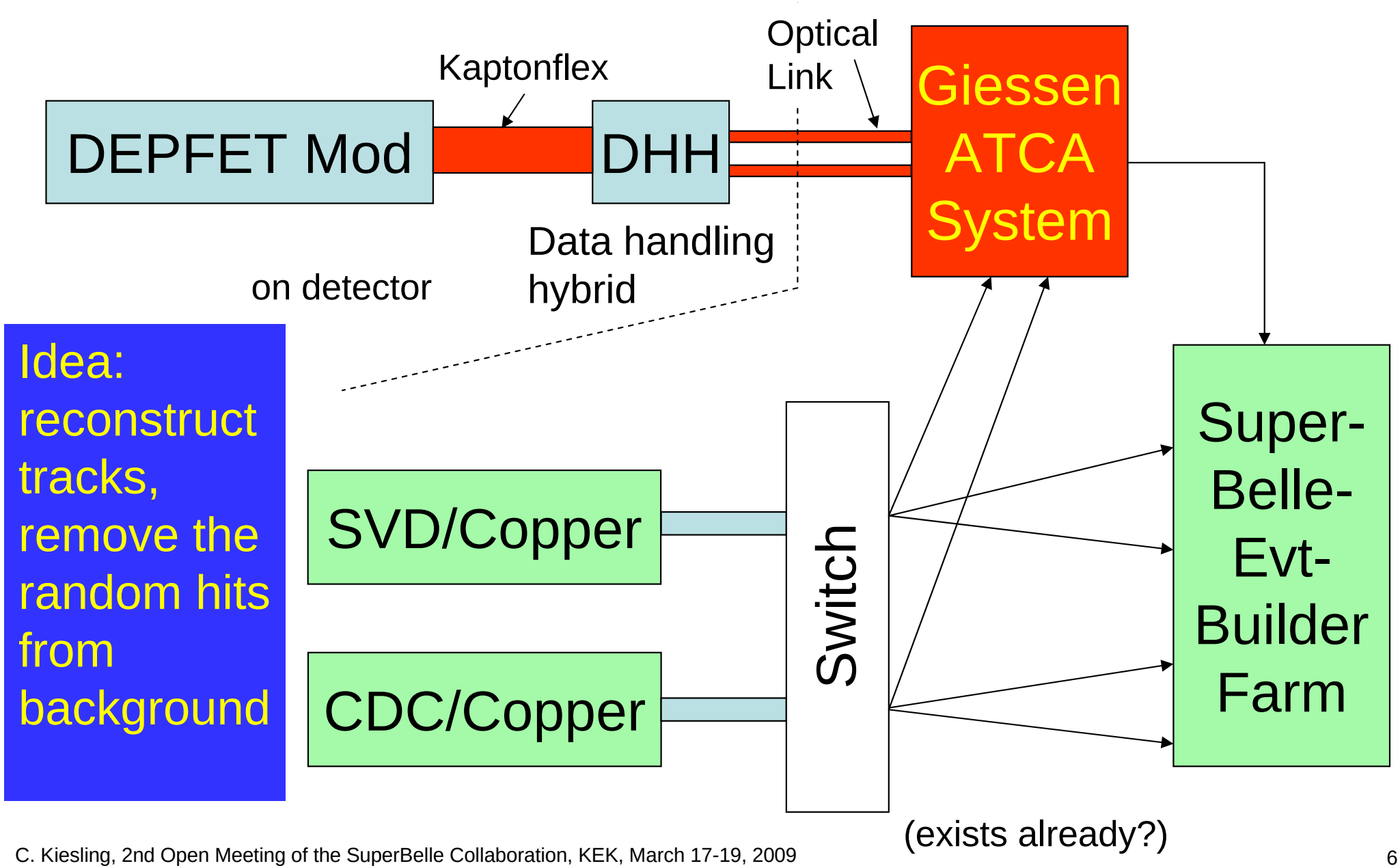
- Data volume:

  → have about 100 k pixels per event (almost all background), about 2 times the data volume of the other subdetectors together

→ need hard thinking how to manage both issues

→ DAQ WP-Meeting at Giessen, Feb 27

Proposal for the PXD DAQ



(see Soeren Lange‘s talk)

ATCA based Compute Node as Backend DAQ for sBelle DEPFET Pixel Detector

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Colleagues involved in project, but not (s)Belle members

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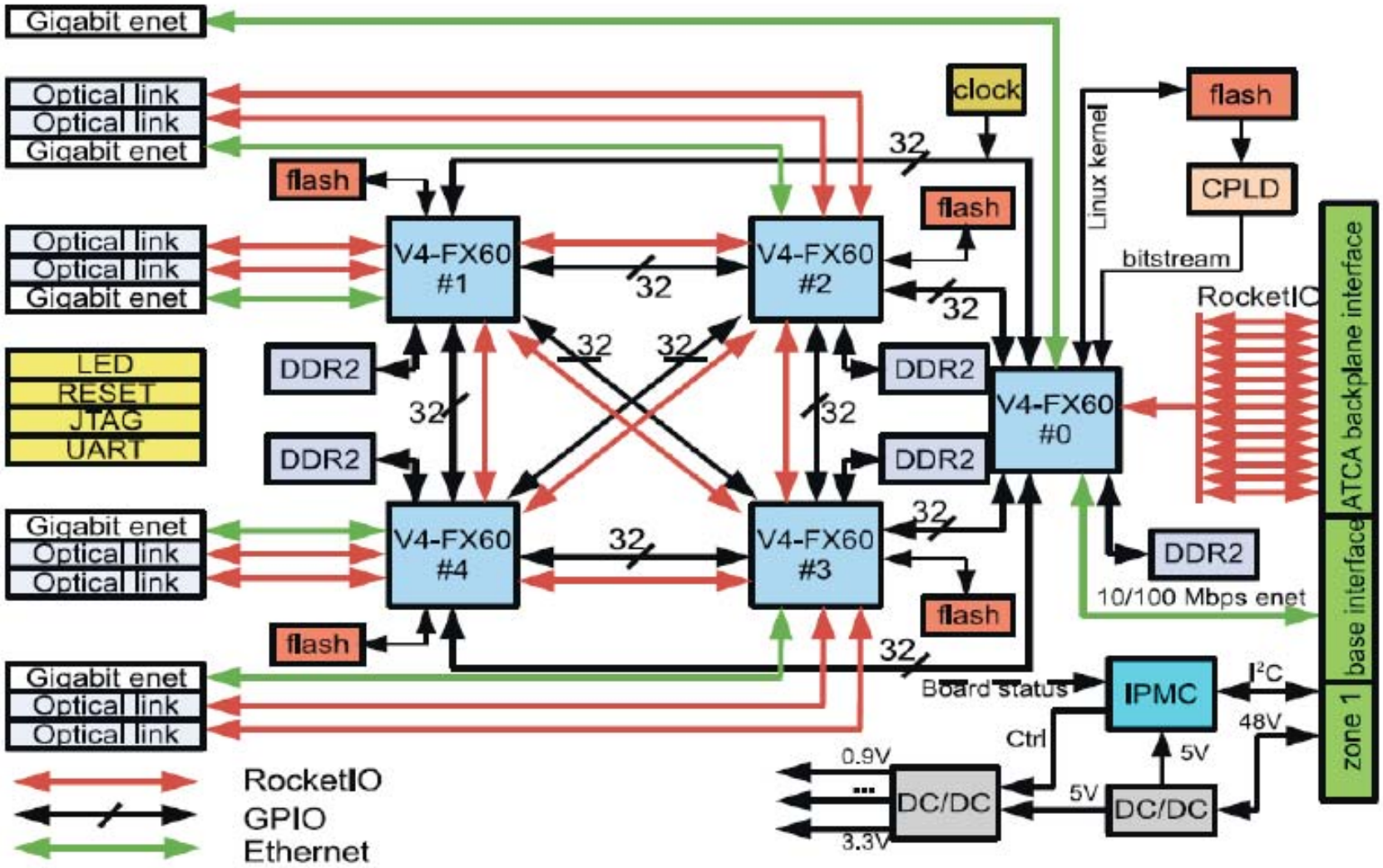
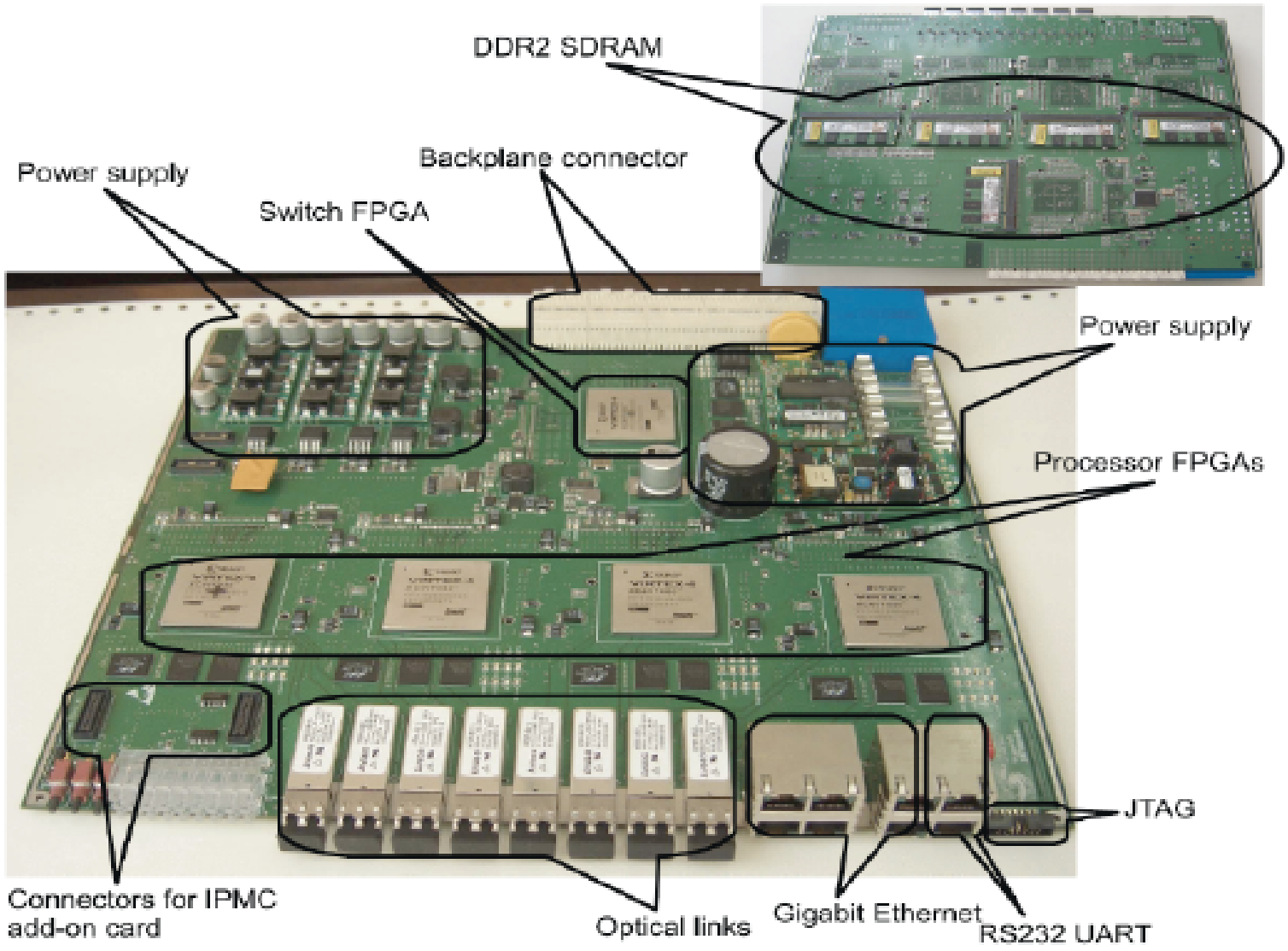
Compute Node (CN) Concept

- **5 x VIRTEX4 FX-60 FPGAs**
  - **each FPGA has 2 x 300 MHz PowerPC**
  - **Linux 2.6.27 (open source version), stored in FLASH memory**
  - **algorithm programming in VHDL (XILINX ISE 10.1)**
- **ATCA (Advanced Telecommunications Computing Architecture) with full mesh backplane (point-to-point connections on backplane from each CN to each other CN, i.e. no bus arbitration)**
- **optical links (connected to RocketIO at FPGA)**
- **Gigabit Ethernet**
- **ATCA management (IPMI) by add-on card**

Compute Node Architecture

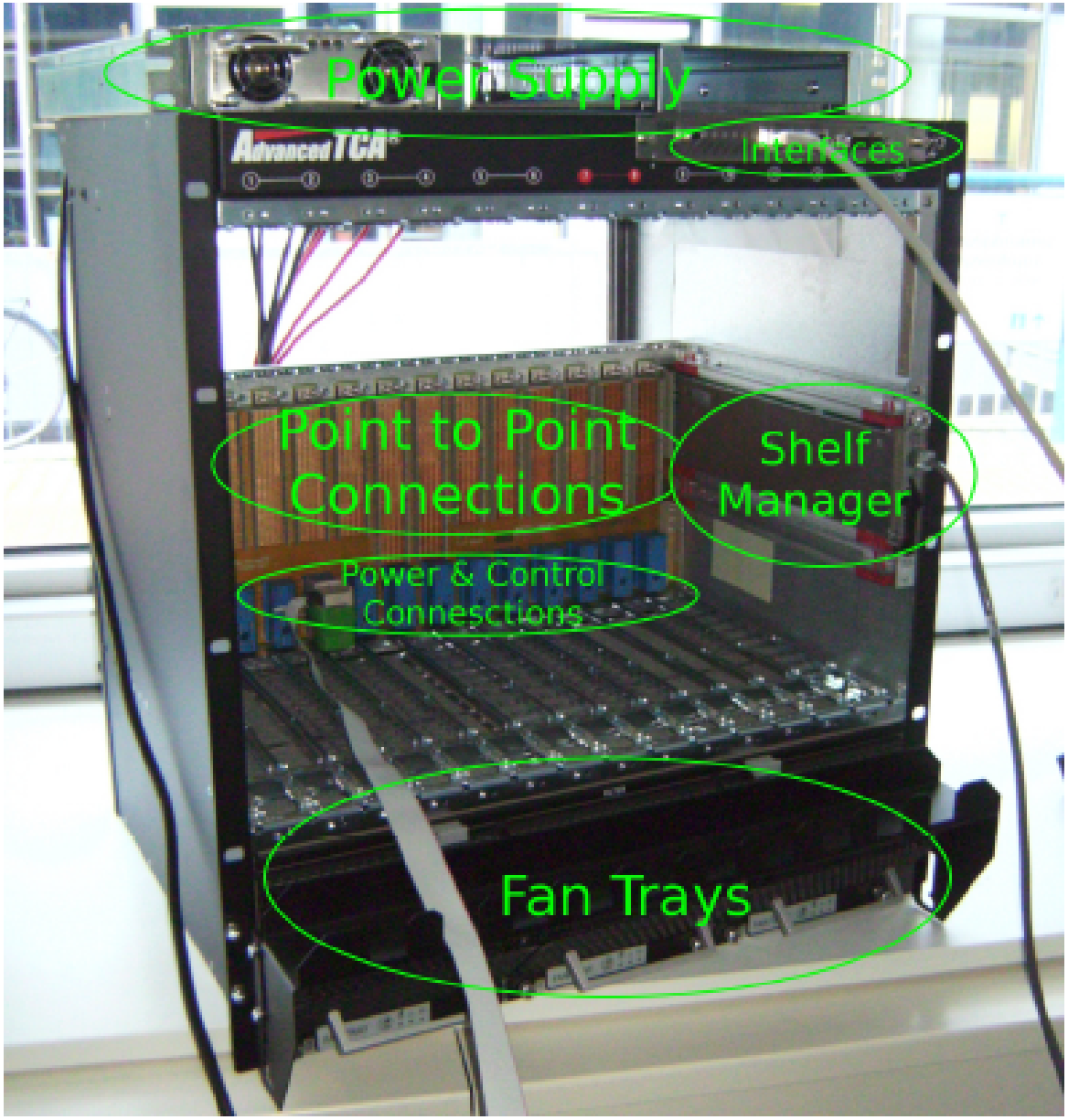


Compute Node (CN)



Proposal for Pixel-Detektor Backend DAQ, Giessen Group

ATCA Shelf


Power Supply
Interfaces
Point to Point Connections
Shelf Manager
Power & Control Connesctions
Fan Trays

Size of the DAQ System

- **Assuming a requirement of 100 Gbit/s for whole pixel detector**
  ATTENTION! Estimate was changed on Valencia meeting, see remarks later (p. 25,26)
- **>> 1 ATCA Shelf with 14 Compute Nodes (+2 spares)**
  - **DATA IN:**
    per 1 compute node 8 optical links @ 1.6 Gbit/s
    x 14 compute nodes per 1 ATCA shelf
    = 180 Gbit/s
    i.e. factor 1.8 safety margin
    DATA OUT:
    5 x GB Ethernet per 1 compute node @ 0.4 GBit/s
  - **150k Euro investment in the BMBF application**
- **This is identical size to system size for the HADES Upgrade (test beamtime at GSI, parallel to existing DAQ system, planned for end of 2009)**
- **Note:**
  the compute note is DAQ prototype system for PANDA (>2016)
  Panda bandwidth requirement is ~10-20% higher than ATLAS
  <3 x 10^7 interactions/s

Conclusion

- PXD will generate a huge amount of data,
  mostly background (~100 k pixels per event, 4bytes each)
  would dominate by far the SuperBelle event size
- No substantial data reduction possible with PXD alone
  (maybe clustering algorithm ~ about factor 2-3)
- Proposal to do fast (FPGA) track reco (using the ATCA system of Giessen) BEFORE the event builders
- Need input from SVD/CDC, similar to Event Builders
- Data reduction by factor 20 or more seems possible